Patent Claims:

1. Circuit arrangement
   - having a flip-flop having a plurality of storage transistors having a threshold voltage of a first value;
   - having a power switch transistor having a threshold voltage of a second value, which is set up in such a way that, by means of the application of a predeterminable electrical potential to its gate terminal, the circuit arrangement can be brought to an operating state in which electric charge carriers contained in the circuit arrangement, in the event of at least one supply voltage being switched off, are protected against flowing away from the circuit arrangement;
   - having a plurality of switching transistors having a threshold voltage of a third value between the flip-flop and the power switch transistor, for coupling a flip-flop input signal into the flip-flop;
   - the first and/or the second value being greater than the third value in terms of magnitude.

2. Circuit arrangement according to Claim 1, in which the flip-flop has two invertors formed from the storage transistors.

3. Circuit arrangement according to Claim 1 or 2, in which a common power switch transistor is provided for the flip-flop and for at least one additional flip-flop.

4. Circuit arrangement according to one of Claims 1 to 3, in which the thickness of the gate-insulating layer of the storage transistors and/or of the power switch transistor is greater than the thickness of the gate-insulating layer of the switching transistors.

5. Circuit arrangement according to one of Claims 1 to 4,
in which the channel width of the storage transistors and/or of the power switch transistor is less than the channel width of the switching transistors.

6. Circuit arrangement according to one of Claims 1 to 5,
in which the switching transistors are connected up in such a way that, in an operating state of the circuit arrangement in which at least one supply voltage of the circuit arrangement is switched off, all the terminals of the switching transistors have a defined electrical potential.

7. Circuit arrangement according to one of Claims 1 to 6,
having at least one second power switch transistor, which is coupled to at least a portion of the switching transistors in such a way that, in an operating state of the circuit arrangement in which at least one supply voltage of the circuit arrangement is switched off, the gate terminals of the switching transistors coupled to the at least one second power switch transistor have a defined electrical potential.

8. Circuit arrangement according to one of Claims 1 to 7,
having at least one third power switch transistor, which is coupled to at least a portion of the switching transistors in such a way that, in an operating state of the circuit arrangement in which at least one supply voltage of the circuit arrangement is switched off, a source/drain terminal of the switching transistors coupled to the at least one third power switch transistor have a defined electrical potential.

9. Circuit arrangement according to Claim 8, in which the at least one third power switch transistor is a p-MOS field-effect transistor.

10. Circuit arrangement according to one of Claims 1 to 9, having a pulse generator circuit for generating a flip-flop input signal from an input signal and from a clock signal, which pulse generator circuit is coupled to the power switch transistor and to the switching transistors.

11. Circuit arrangement according to Claim 10, in which the pulse generator circuit has a plurality of pulse generator transistors having a fourth value of the threshold voltage, the first and/or the second value being greater than the fourth value in terms of magnitude.

12. Circuit arrangement according to Claim 10 or 11, in which the pulse generator circuit has a logic subcircuit for generating at least one flip-flop input signal from at least one input signal in accordance with a predeterminable logic operation.

13. Circuit arrangement according to Claim 12, in which the logic subcircuit is set up in such a way that the logic operation is an

- inverter operation;
- AND operation;
- OR operation;
- NAND operation;
- NOR operation; or
- exclusive-OR operation;
- exclusive-NOR operation.

14. Circuit arrangement according to Claim 12 or 13,

in which the logic subcircuit has a plurality of logic transistors having a fifth value of the threshold voltage, the first and/or the second value being greater than the fifth value in terms of magnitude.

15. Circuit arrangement according to one of Claims 1 to 14,
having a control unit for controlling supply voltages which can be applied to terminals of at least a portion of the transistors of the circuit arrangement, which control unit is set up in such a way that, in an energy-saving operating state, it can switch off all the supply voltages with the exception of supply voltages of the flip-flop.

16. Circuit arrangement according to one of Claims 1 to 15,
having a test circuit coupled to the flip-flop, which test circuit is set up for testing the functionality of the flip-flop.

17. Circuit arrangement according to Claim 16,
in which the test circuit has an input component, set up for programming a test input signal into the flip-flop, and an output component, set up for reading out a test output signal from the flip-flop.

18. Circuit arrangement according to Claim 16 or 17,
in which the test circuit has a plurality of test transistors having a sixth value of the threshold voltage, the sixth value being greater than at least one of the third to fifth values in terms of magnitude.

19. Circuit arrangement according to Claim 18,
in which the test transistors have a gate-insulating layer having a greater thickness than the thickness of the gate-insulating layer of the switching transistors

and/or of the pulse generator transistors and/or of the logic transistors.

20. Circuit arrangement according to one of Claims 1 to 19,
having one or more protection transistors having a threshold voltage of a seventh value between the flip-flop and the switching transistors, which protection transistors are connected up for selectively coupling or decoupling flip-flop and switching transistors, the seventh value being greater than the third value in terms of magnitude.

21. Circuit arrangement according to Claim 20,
in which the protection transistors have a gate-insulating layer having a greater thickness than the thickness of the gate-insulating layer of the switching transistors and/or of the pulse generator transistors and/or of the logic transistors.

22. Circuit arrangement according to Claim 20 or 21,
which is set up in such a way that

- in a first operating state, in which at least one supply voltage of the circuit arrangement is switched off, by means of electrical control signals being prescribed to at least a portion of the protection transistors, the latter electrically decouple flip-flop and switching transistors from one another;
- in a second operating state, in which the circuit arrangement is supplied with supply voltages, by means of electrical control signals being prescribed to at least a portion of the switching transistors, the latter electrically couple flip-flop and switching transistors to one another.

23. Circuit arrangement according to one of Claims 20 to 22,
in which the protection transistors have at least one transistor pair of transistors of different conduction types which are connected in parallel with one another, which at least one transistor pair is connected by its source/drain terminals between flip-flop and switching transistors.

List of Reference Symbols

100	Circuit arrangement
101	CMOS circuit
102	Power switch circuit
103	First field-effect transistor
104	Second field-effect transistor
105	Supply voltage
106	Ground potential
107	Standby voltage
108	Active state voltage
200	Low threshold voltage n-MOS field-effect transistor
201	High threshold voltage n-MOS field-effect transistor
202	Low threshold voltage p-MOS field-effect transistors
203	High threshold voltage p-MOS field-effect transistor
300	Circuit arrangement
301	Flip-flop subcircuit
302	Pulse generator subcircuit
303	Power switch subcircuit
304	Coupling-in subcircuit
305	Clock input
306	First n-MOS pulse generator transistor
307	First p-MOS pulse generator transistor
308	Second p-MOS pulse generator transistor
309	Third p-MOS pulse generator transistor
310	Fourth p-MOS pulse generator transistor
311	Supply voltage
312	Second n-MOS pulse generator trnasisotr
313	Third n-MOS pulse generator transistor
314	Fourth n-MOS pulse generator transistor
315	Fourth n-MOS pulse generator transistor
316	Fifth n-MOS pulse generator transistor
317	First power switch transistor
318	Ground potential

319 First p-MOS switching transistor
320 Second p-MOS switching transistor
321 First n-MOS switching transistor
322 Second n-MOS switching transistor
323 Third p-MOS switching transistor
324 Third n-MOS switching transistor
325 Fourth p-MOS switching transistor
326 Fourth n-MOS switching transistor
327 First p-MOS storage transistor
328 First n-MOS storage transistor
329 Second p-MOS storage transistor
330 Second n-MOS storage transistor
400 Circuit arrangement
401 Reference potential circuit
402 First n-MOS reference potential transistor
403 Second n-MOS reference potential transistor
500 Circuit arrangement
501 Reference potential circuit
502 Second power switch trnasisotr
600 Circuit arrangement
601 Reference potential circuit
602 Third power switch transistor
700 Circuit arrangement
701 Scan path subcircuit
702 First n-MOS scan path transistor
703 Second n-MOS scan path transistor
704 Third n-MOS scan path transistor
705 Fourth n-MOS scan path transistor
706 First p-MOS scan path transistor
707 Second p-MOS scan path transistor
708 Fifth n-MOS scan path transistor
709 Sixth n-MOS scan path transistor
710 Third p-MOS scan path transistor
711 Fourth p-MOS scan path transistor
712 Seventh n-MOS scan path transistor
713 Eighth n-MOS scan path transistor
714 Fifth p-MOS scan path transistor
715 Sixth p-MOS scan path transistor

716 Ninth n-MOS scan path transistor
717 Tenth n-MOS scan path transistor
800 Circuit arrangement
801 Pulse generator subcircuit
802 First n-MOS logic transistor
803 Second n-MOS logic transistor
804 Third n-MOS logic transistor
805 Fourth n-MOS logic transistor
806 Fifth n-MOS logic transistor
807 Sixth n-MOS logic transistor
900 Circuit arrangement
901 First transmission gate subcircuit
902 Second transmission gate subcircuit
903 First p-MOS protection transistor
904 First n-MOS protection transistor
905 Second p-MOS protection transistor
906 Second n-MOS protection transistor
1100 Timing diagram
1101 Time axis
1102 Signal axis